WHAT IS CLAIMED IS:

1. A device for generating a clock signal and decoding data for use in a contactless integrated circuit device comprising:

a receiver for receiving a radio frequency (RF) signal having a pause period;

a divider for dividing the received RF signal to provide a divided signal;

a first counter for counting a period of the divided signal at each non-pause period of the received RF signal;

a second counter for counting a period of the divided signal; and

a decoder for generating a synchronous clock signal and a decoded data signal in response to outputs of the first and second counters.

2. The device according to claim 1, wherein the first counter is reset during the pause period of the RF signal.

3. The device according to claim 1, wherein the second counter is reset at a falling edge of the synchronous clock signal.

4. The device according to claim 1, wherein the RF signal is based on an ISO-14443 Type A interface.

5. The device according to claim 4, wherein the decoder further generates a signal indicating an end of a received frame in response to the outputs of the first and second counters.

6. A data restoring device for use in a contactless integrated circuit card comprising:

a receiver for receiving an RF signal having a pause period and extracting data and clock signals from the received RF signal;

a divider for dividing the clock signal to generate a divided clock signal;

a first counter for counting a period of the divided clock signal at each non-pause period of the data signal;

a second counter for counting a period of the divided clock signal; and

a decoder for generating a synchronous clock signal and a decoded data signal in response to outputs of the first and second counters.

7. The device according to claim 6, wherein the first counter is

reset at a start of the pause period of the data signal.

8. The device according to claim 7, wherein the first counter is a 3-bit counter.

9. The device according to claim 6, wherein the second counter is reset in response to the synchronous clock signal.

10. The device according to claim 9, wherein the second counter is reset at a falling edge of the synchronous clock signal.

11. The device according to claim 9, wherein the second counter is a 2-bit counter.

12. The device according to claim 10, wherein an output of the second counter sequentially varies between '0' and '2'.

13. The device according to claim 6, wherein the first counter is a 4-bit counter.

14. The device according to claim 13, wherein the second counter is reset by a combination of the outputs of the first and second counters.

15. The device according to claim 6, wherein the second counter is a 3-bit counter.

16. The device according to claim 6, wherein the RF signal is based on an ISO-14443 A-Type interface.

17. The device according to claim 16, wherein the decoder further generates a signal indicating an end of a received frame in response to the outputs of the first and second counters.

18. The device according to claim 6, further comprising an OR gate for receiving a reset signal for resetting the card and the data signal, wherein the first counter is reset by an output of the OR gate.

19. The device according to claim 6, wherein the divider includes:

a plurality of division units connected in series between an input terminal and an output terminal, wherein the input terminal receives the clock signal from the receiver and each division unit divides an input signal by N (N is an integer); and

a selector for selecting one of outputs of the division units in response to an external selection signal, as the divided clock signal.